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## ##

## C A L I B R E S Y S T E M ##

## ##

## L V S R E P O R T ##

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REPORT FILE NAME: sr\_latch.lvs.report

LAYOUT NAME: /afs/iitd.ac.in/user/e/ee/een212026/ieclab\_21/lvs/sr\_latch.sp ('sr\_latch')

SOURCE NAME: /afs/iitd.ac.in/user/e/ee/een212026/ieclab\_21/lvs/sr\_latch.src.net ('sr\_latch')

RULE FILE: /afs/iitd.ac.in/user/e/ee/een212026/ieclab\_21/lvs/\_\_\_\_G-DF-LOGIC\_MIXED\_MODE65N-LL\_LOW\_K\_CALIBRE-LVS-1.6-P4.txt\_\_\_\_

RULE FILE TITLE: UMC Calibre LVS 65nm LOGIC/MIXED MODE Low Leakage Low-K Process

CREATION TIME: Fri Sep 17 23:09:18 2021

CURRENT DIRECTORY: /afs/iitd.ac.in/user/e/ee/een212026/ieclab\_21/lvs

USER NAME: een212026

CALIBRE VERSION: v2020.4\_34.17 Tue Dec 1 16:11:11 PST 2020

OVERALL COMPARISON RESULTS

# ################### \_ \_

# # # \* \*

# # # CORRECT # |

# # # # \\_\_\_/

# ###################

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CELL SUMMARY

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Result Layout Source

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CORRECT sr\_latch sr\_latch

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LVS PARAMETERS

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o LVS Setup:

// LVS COMPONENT TYPE PROPERTY

// LVS COMPONENT SUBTYPE PROPERTY

// LVS PIN NAME PROPERTY

LVS POWER NAME "?VCC?" "?VDD?"

LVS GROUND NAME "?GND?" "?VSS?"

LVS CELL SUPPLY NO

LVS RECOGNIZE GATES ALL

// LVS HCELL REPORT

LVS IGNORE PORTS NO

LVS CHECK PORT NAMES YES

LVS IGNORE TRIVIAL NAMED PORTS NO

LVS BUILTIN DEVICE PIN SWAP NO

LVS ALL CAPACITOR PINS SWAPPABLE NO

LVS DISCARD PINS BY DEVICE NO

LVS SOFT SUBSTRATE PINS NO

LVS INJECT LOGIC NO

LVS EXPAND UNBALANCED CELLS YES

LVS FLATTEN INSIDE CELL NO

LVS EXPAND SEED PROMOTIONS YES

LVS PRESERVE PARAMETERIZED CELLS NO

LVS GLOBALS ARE PORTS YES

LVS REVERSE WL NO

LVS SPICE PREFER PINS NO

LVS SPICE SLASH IS SPACE YES

LVS SPICE ALLOW FLOATING PINS YES

// LVS SPICE ALLOW INLINE PARAMETERS

LVS SPICE ALLOW UNQUOTED STRINGS NO

LVS SPICE CONDITIONAL LDD NO

LVS SPICE CULL PRIMITIVE SUBCIRCUITS NO

// LVS SPICE EXCLUDE CELL SOURCE

// LVS SPICE EXCLUDE CELL LAYOUT

LVS SPICE IMPLIED MOS AREA NO

// LVS SPICE MULTIPLIER NAME

LVS SPICE OVERRIDE GLOBALS NO

LVS SPICE REDEFINE PARAM NO

LVS SPICE REPLICATE DEVICES YES

LVS SPICE SCALE X PARAMETERS NO

LVS SPICE STRICT WL NO

// LVS SPICE OPTION

LVS STRICT SUBTYPES NO

LVS EXACT SUBTYPES NO

LAYOUT CASE NO

SOURCE CASE NO

LVS COMPARE CASE NO

LVS COMPARE CASE STRICT NO

LVS DOWNCASE DEVICE NO

LVS REPORT MAXIMUM 50

LVS PROPERTY RESOLUTION MAXIMUM 32

// LVS SIGNATURE MAXIMUM

// LVS FILTER UNUSED OPTION

// LVS REPORT OPTION

LVS REPORT UNITS YES

// LVS NON USER NAME PORT

// LVS NON USER NAME NET

// LVS NON USER NAME INSTANCE

// LVS IGNORE DEVICE PIN

// LVS PREFER NETS FILTER SOURCE

// LVS PREFER NETS FILTER LAYOUT

LVS PREFER PORT NETS NO

LVS EXPAND ON ERROR NO

// Reduction

LVS REDUCE SERIES MOS NO

LVS REDUCE PARALLEL MOS YES

LVS REDUCE SEMI SERIES MOS NO

LVS REDUCE SPLIT GATES YES

LVS REDUCE PARALLEL BIPOLAR YES

LVS REDUCE SERIES CAPACITORS YES

LVS REDUCE PARALLEL CAPACITORS YES

LVS REDUCE SERIES RESISTORS YES

LVS REDUCE PARALLEL RESISTORS YES

LVS REDUCE PARALLEL DIODES YES

LVS REDUCE C(MIMCAPS\_20F\_MM) PARALLEL NO

LVS REDUCE C(NCAP\_12\_LL) PARALLEL NO

LVS REDUCE C(PCAP\_12\_LL) PARALLEL NO

LVS REDUCE C(NCAP\_25\_LL) PARALLEL NO

LVS REDUCE C(PCAP\_25\_LL) PARALLEL NO

LVS REDUCTION PRIORITY PARALLEL

LVS SHORT EQUIVALENT NODES NO

// Trace Property

TRACE PROPERTY n\_12\_llrvtrf lf lf 3

TRACE PROPERTY n\_12\_llrvtrf wf wf 3

TRACE PROPERTY n\_12\_llrvtrf nf nf 0

TRACE PROPERTY n\_12\_llrvtrf con con 0

TRACE PROPERTY p\_12\_llrvtrf lf lf 3

TRACE PROPERTY p\_12\_llrvtrf wf wf 3

TRACE PROPERTY p\_12\_llrvtrf nf nf 0

TRACE PROPERTY p\_12\_llrvtrf con con 0

TRACE PROPERTY n\_bpw\_12\_llrvtrf lf lf 3

TRACE PROPERTY n\_bpw\_12\_llrvtrf wf wf 3

TRACE PROPERTY n\_bpw\_12\_llrvtrf nf nf 0

TRACE PROPERTY n\_bpw\_12\_llrvtrf con con 0

TRACE PROPERTY n\_12\_llhvtrf lf lf 3

TRACE PROPERTY n\_12\_llhvtrf wf wf 3

TRACE PROPERTY n\_12\_llhvtrf nf nf 0

TRACE PROPERTY n\_12\_llhvtrf con con 0

TRACE PROPERTY p\_12\_llhvtrf lf lf 3

TRACE PROPERTY p\_12\_llhvtrf wf wf 3

TRACE PROPERTY p\_12\_llhvtrf nf nf 0

TRACE PROPERTY p\_12\_llhvtrf con con 0

TRACE PROPERTY n\_bpw\_12\_llhvtrf lf lf 3

TRACE PROPERTY n\_bpw\_12\_llhvtrf wf wf 3

TRACE PROPERTY n\_bpw\_12\_llhvtrf nf nf 0

TRACE PROPERTY n\_bpw\_12\_llhvtrf con con 0

TRACE PROPERTY n\_12\_lllvtrf lf lf 3

TRACE PROPERTY n\_12\_lllvtrf wf wf 3

TRACE PROPERTY n\_12\_lllvtrf nf nf 0

TRACE PROPERTY n\_12\_lllvtrf con con 0

TRACE PROPERTY p\_12\_lllvtrf lf lf 3

TRACE PROPERTY p\_12\_lllvtrf wf wf 3

TRACE PROPERTY p\_12\_lllvtrf nf nf 0

TRACE PROPERTY p\_12\_lllvtrf con con 0

TRACE PROPERTY n\_bpw\_12\_lllvtrf lf lf 3

TRACE PROPERTY n\_bpw\_12\_lllvtrf wf wf 3

TRACE PROPERTY n\_bpw\_12\_lllvtrf nf nf 0

TRACE PROPERTY n\_bpw\_12\_lllvtrf con con 0

TRACE PROPERTY n\_25\_llrf lf lf 3

TRACE PROPERTY n\_25\_llrf wf wf 3

TRACE PROPERTY n\_25\_llrf nf nf 0

TRACE PROPERTY n\_25\_llrf con con 0

TRACE PROPERTY p\_25\_llrf lf lf 3

TRACE PROPERTY p\_25\_llrf wf wf 3

TRACE PROPERTY p\_25\_llrf nf nf 0

TRACE PROPERTY p\_25\_llrf con con 0

TRACE PROPERTY n\_bpw\_25\_llrf lf lf 3

TRACE PROPERTY n\_bpw\_25\_llrf wf wf 3

TRACE PROPERTY n\_bpw\_25\_llrf nf nf 0

TRACE PROPERTY n\_bpw\_25\_llrf con con 0

TRACE PROPERTY r(rsnpo\_efuse) r r 3

TRACE PROPERTY r(rsppo\_efuse) r r 3

TRACE PROPERTY rnnpo\_nw\_llrf r r 3

TRACE PROPERTY rnnpo\_nw\_llrf l l 3

TRACE PROPERTY rnnpo\_nw\_llrf w w 3

TRACE PROPERTY rnnpo\_llrf r r 3

TRACE PROPERTY rnnpo\_llrf l l 3

TRACE PROPERTY rnnpo\_llrf w w 3

TRACE PROPERTY rnppo\_nw\_llrf r r 3

TRACE PROPERTY rnppo\_nw\_llrf l l 3

TRACE PROPERTY rnppo\_nw\_llrf w w 3

TRACE PROPERTY rnppo\_llrf r r 3

TRACE PROPERTY rnppo\_llrf l l 3

TRACE PROPERTY rnppo\_llrf w w 3

TRACE PROPERTY rnhr\_nw\_llrf r r 3

TRACE PROPERTY rnhr\_nw\_llrf l l 3

TRACE PROPERTY rnhr\_nw\_llrf w w 3

TRACE PROPERTY rnhr\_llrf r r 3

TRACE PROPERTY rnhr\_llrf l l 3

TRACE PROPERTY rnhr\_llrf w w 3

TRACE PROPERTY r(fuse) r r 3

TRACE PROPERTY r(ral) r r 3

TRACE PROPERTY varmis\_12\_llrf lf lf 3

TRACE PROPERTY varmis\_12\_llrf wf wf 3

TRACE PROPERTY varmis\_12\_llrf nf nf 0

TRACE PROPERTY varmis\_12\_llrf array array 0

TRACE PROPERTY varmis\_25\_llrf lf lf 3

TRACE PROPERTY varmis\_25\_llrf wf wf 3

TRACE PROPERTY varmis\_25\_llrf nf nf 0

TRACE PROPERTY varmis\_25\_llrf array array 0

TRACE PROPERTY vardiop\_llrf l l 3

TRACE PROPERTY vardiop\_llrf wp wp 3

TRACE PROPERTY vardiop\_llrf nf nf 0

TRACE PROPERTY vardiop\_llrf c c 3

TRACE PROPERTY d(dionw\_ll) a a 3

TRACE PROPERTY d(dionw\_ll) p p 3

TRACE PROPERTY d(diodnw\_ll) a a 3

TRACE PROPERTY d(diodnw\_ll) p p 3

TRACE PROPERTY d(diodp\_ll) a a 3

TRACE PROPERTY d(diodp\_ll) p p 3

TRACE PROPERTY momcaps\_sy\_mmkf nf nf 0

TRACE PROPERTY momcaps\_sy\_mmkf l l 3

TRACE PROPERTY momcaps\_sy\_mmkf nm nm 0

TRACE PROPERTY momcaps\_sy\_mmkf bm bm 0

TRACE PROPERTY momcaps\_as\_mmkf nf nf 0

TRACE PROPERTY momcaps\_as\_mmkf l l 3

TRACE PROPERTY momcaps\_as\_mmkf nm nm 0

TRACE PROPERTY momcaps\_as\_mmkf bm bm 0

TRACE PROPERTY momcaps\_symesh\_mmkf nf nf 0

TRACE PROPERTY momcaps\_symesh\_mmkf mh mh 0

TRACE PROPERTY momcaps\_symesh\_mmkf nm nm 0

TRACE PROPERTY momcaps\_symesh\_mmkf bm bm 0

TRACE PROPERTY momcaps\_symesh\_mmkf l l 3

TRACE PROPERTY momcaps\_asmesh\_mmkf nf nf 0

TRACE PROPERTY momcaps\_asmesh\_mmkf mh mh 0

TRACE PROPERTY momcaps\_asmesh\_mmkf nm nm 0

TRACE PROPERTY momcaps\_asmesh\_mmkf bm bm 0

TRACE PROPERTY momcaps\_asmesh\_mmkf l l 3

TRACE PROPERTY momcaps\_array\_vp3\_rfvcl bm bm 0

TRACE PROPERTY momcaps\_array\_vp3\_rfvcl ns ns 0

TRACE PROPERTY momcaps\_array\_vp3\_rfvcl nf nf 0

TRACE PROPERTY momcaps\_array\_vp3\_rfvcl array array 0

TRACE PROPERTY momcaps\_array\_vp3\_rfvcl lf lf 3

TRACE PROPERTY momcaps\_array\_vp4\_rfvcl bm bm 0

TRACE PROPERTY momcaps\_array\_vp4\_rfvcl ns ns 0

TRACE PROPERTY momcaps\_array\_vp4\_rfvcl nf nf 0

TRACE PROPERTY momcaps\_array\_vp4\_rfvcl array array 0

TRACE PROPERTY momcaps\_array\_vp4\_rfvcl lf lf 3

TRACE PROPERTY momcaps\_array\_vp5\_rfvcl bm bm 0

TRACE PROPERTY momcaps\_array\_vp5\_rfvcl ns ns 0

TRACE PROPERTY momcaps\_array\_vp5\_rfvcl nf nf 0

TRACE PROPERTY momcaps\_array\_vp5\_rfvcl array array 0

TRACE PROPERTY momcaps\_array\_vp5\_rfvcl lf lf 3

TRACE PROPERTY momcaps\_array\_vp5\_rfvcl sh sh 0

TRACE PROPERTY l\_slcr30k\_rfvil s s 3

TRACE PROPERTY l\_slcr30k\_rfvil w w 3

TRACE PROPERTY l\_slcr30k\_rfvil od od 3

TRACE PROPERTY l\_slcr30k\_rfvil nt nt 0

TRACE PROPERTY l\_syct30k\_rfvil nt nt 0

TRACE PROPERTY l\_syct30k\_rfvil s s 3

TRACE PROPERTY l\_syct30k\_rfvil w w 3

TRACE PROPERTY l\_syct30k\_rfvil od od 3

TRACE PROPERTY l\_sy30k\_rfvil nt nt 0

TRACE PROPERTY l\_sy30k\_rfvil s s 3

TRACE PROPERTY l\_sy30k\_rfvil w w 3

TRACE PROPERTY l\_sy30k\_rfvil od od 3

TRACE PROPERTY l\_sqsk\_rfvil nt nt 0

TRACE PROPERTY l\_sqsk\_rfvil s s 3

TRACE PROPERTY l\_sqsk\_rfvil w w 3

TRACE PROPERTY l\_sqsk\_rfvil od od 3

TRACE PROPERTY l\_sqsk\_rfvil ns ns 0

TRACE PROPERTY l\_sqsk\_rfvil bm bm 0

TRACE PROPERTY mimcaps\_20f\_nwell\_rfkf l l 3

TRACE PROPERTY mimcaps\_20f\_nwell\_rfkf w w 3

TRACE PROPERTY mimcaps\_20f\_psub\_rfkf l l 3

TRACE PROPERTY mimcaps\_20f\_psub\_rfkf w w 3

TRACE PROPERTY mimcaps\_20f\_m1\_rfkf l l 3

TRACE PROPERTY mimcaps\_20f\_m1\_rfkf w w 3

TRACE PROPERTY c(mimcaps\_20f\_mm) c c 3

TRACE PROPERTY l\_sq\_trans\_rfvil nt\_in nt\_in 0

TRACE PROPERTY l\_sq\_trans\_rfvil nt\_out nt\_out 0

TRACE PROPERTY l\_sq\_trans\_rfvil w w 3

TRACE PROPERTY l\_sq\_trans\_rfvil od od 3

TRACE PROPERTY l\_sqctin\_trans\_rfvil nt\_in nt\_in 0

TRACE PROPERTY l\_sqctin\_trans\_rfvil nt\_out nt\_out 0

TRACE PROPERTY l\_sqctin\_trans\_rfvil w w 3

TRACE PROPERTY l\_sqctin\_trans\_rfvil od od 3

TRACE PROPERTY l\_sqctout\_trans\_rfvil nt\_in nt\_in 0

TRACE PROPERTY l\_sqctout\_trans\_rfvil nt\_out nt\_out 0

TRACE PROPERTY l\_sqctout\_trans\_rfvil w w 3

TRACE PROPERTY l\_sqctout\_trans\_rfvil od od 3

TRACE PROPERTY l\_sqctinout\_trans\_rfvil nt\_in nt\_in 0

TRACE PROPERTY l\_sqctinout\_trans\_rfvil nt\_out nt\_out 0

TRACE PROPERTY l\_sqctinout\_trans\_rfvil w w 3

TRACE PROPERTY l\_sqctinout\_trans\_rfvil od od 3

TRACE PROPERTY l\_occtout\_trans\_rfvil nt\_in nt\_in 0

TRACE PROPERTY l\_occtout\_trans\_rfvil w w 3

TRACE PROPERTY l\_occtout\_trans\_rfvil od od 3

TRACE PROPERTY pad\_rf index\_layer index\_layer 0

TRACE PROPERTY pad\_rf index\_thick index\_thick 0

TRACE PROPERTY pad\_rf index\_pad index\_pad 0

CELL COMPARISON RESULTS ( TOP LEVEL )

# ################### \_ \_

# # # \* \*

# # # CORRECT # |

# # # # \\_\_\_/

# ###################

LAYOUT CELL NAME: sr\_latch

SOURCE CELL NAME: sr\_latch

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INITIAL NUMBERS OF OBJECTS

--------------------------

Layout Source Component Type

------ ------ --------------

Ports: 6 6

Nets: 8 8

Instances: 4 4 MN (4 pins)

4 4 MP (4 pins)

------ ------

Total Inst: 8 8

NUMBERS OF OBJECTS AFTER TRANSFORMATION

---------------------------------------

Layout Source Component Type

------ ------ --------------

Ports: 6 6

Nets: 6 6

Instances: 2 2 NAND2 (3 pins)

------ ------

Total Inst: 2 2

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INFORMATION AND WARNINGS

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Matched Matched Unmatched Unmatched Component

Layout Source Layout Source Type

------- ------- --------- --------- ---------

Ports: 6 6 0 0

Nets: 6 6 0 0

Instances: 2 2 0 0 NAND2

------- ------- --------- ---------

Total Inst: 2 2 0 0

o Initial Correspondence Points:

Ports: VDD GND S QBAR Q R

o Voltage Names Matched by Wildcard:

Power Names from Layout:

VDD

Ground Names from Layout:

GND

Power Names from Source:

VDD

Ground Names from Source:

GND

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SUMMARY

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Total CPU Time: 0 sec

Total Elapsed Time: 0 sec